Amendments to the Specification

On page 10, third paragraph, please make changes, as shown.

The gate region 174 and the drain region 173 are provided with layers of tungsten silicide and ~~tungsten plugs 122~~ tungsten plugs 122a and 122b for electrically connecting the gate region 174 and the drain region 173 to the selection lines 121 and 120, respectively. The selection lines 120 and 121 are formed from a conductive material such as, e.g., aluminum or copper. The source region 172 is provided with a layer of tungsten silicide and a tungsten plug as well.

On page 11, second paragraph, please make changes, as shown.

Onto layer 107 or, if present, onto layer 110, masks 111 and 112 are formed by, e.g., lithography or electron beam writing. Masks 111 each cover parts of layer 107 and layer 110, if present, which cover the respective electric conductors 124. Masks 112 cover other parts of layer 107 and layer 110, if present, onto which further ~~electric conductors 125 will be~~ electric conductors (not illustrated) will be formed later on. For every memory element, masks 111 and 112 are separated by a distance L which is typically below 300 nm and preferably between 20 and 200 nm. When lithography is used to form the mask 111 and the mask 112, the minimum distance L is preferably approximately equal to the minimum dimension achievable by lithography. The shorter the distance L the smaller the electric power required to induce a phase transition between the first and the second phase. The distance L determines the length of the phase change material, which will have a cross-section smaller than the phase change material at the electric conductors 124 as will be described below. The phase change material having the reduced cross-section is referred to as the volume of the phase change material.

On page 11, third paragraph, please make changes as shown.

The parts of layer 110, if present, that are not covered by masks 111 and 112 are removed by isotropic etching using, e.g., a solution comprising HF. The result obtained at this stage of the process of manufacturing the electric device 100 is shown in Fig. 4. Note that due to the isotropic etching ~~an undereteh occurs,~~ an undercut occurs, see Figs. 4 and 5. Then the parts of layer 107 not covered by masks 111 and 112 are anisotropically etched, using, e.g., a reactive ion etch comprising Cl. As a result sidewall spacers composed of the phase change material are formed

inside the openings 108 at the position not covered by masks 111 and 112. This implies reducing a cross-section of a conductive path in the layer 107 between the first contact area covered by mask 111 and a second contact area covered by mask 112. The cross-section is smaller than the first contact area and the second contact area. For each memory element 170 the sidewall spacers formed by layer 107 are electrically connected to those parts of layer 107 and layer 110, if present, which were covered by masks 111 and 112 during the etching step. As shown in the cross-section of Fig. 6 the sidewall spacers formed of layer 107 have a width W that is substantially equal to the thickness LT of layer 107. In